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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/589,621	06/07/2000	Sara Ruhina Biyabani	004860.P2438	8620

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EXAMINER	
CASCHERA, ANTONIO A	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 11/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/589,621	BIYABANI, SARA RUHINA	
	Examiner	Art Unit	
	Antonio A Caschera	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 2 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Rao (WO 97/06523).

In reference to claims 1 and 2, Rao discloses a processing system including a unified system/frame buffer memory collocated in a single integrated circuit or bank of circuits (see page 6, lines 18-22). Rao discloses a core logic unit that exchanges data, addresses and instructions between a CPU, display controller and the unified memory (see pages 11-12, lines 33-2). Rao further discloses that the core logic unit may be any of a number of commercially available logic chips (see page 12, lines 3-6) which the office interprets as functionally equivalent to the memory controller of applicant's claim. Rao discloses the core logic unit connected to main memory, the display subsystem and CPU (see interconnections between core logic (#103), CPU (101) and display controller (104) of Figure 1). Rao discloses the unified memory being partitioned into a system memory and a display frame buffer which is further divided into first and second frame buffer blocks (see page 13, lines 13-16 and #105, 109-111 of Figure 1). Rao further discloses one of the two frame buffer blocks to function as "refresh" memory and the other block to function as a "screen update" memory (see pages 13-14, lines 35-1 and page 14,

lines 22-23) which the office interpret as functionally equivalent to the "refresh" and "frame preparation" memories respectively, of applicant's claim. Rao further discloses that the "screen update" and "refresh" memories are role reversed so that the previous "screen update" block now becomes the "refresh" block and the previous "refresh" block now becomes the "frame preparation" block (see page 15, lines 8-16), therefore the office interprets that each memory block is connected to both the display controller and display device. Rao also discloses each block of memory to comprise of pixel data (see page 13, lines 30-32) which the office interprets equivalent to color data. Rao discloses data being written to the "screen update" memory using one CPU cycle for each word of data being written (see page 14, lines 32-34). Rao further discloses the display controller writing refresh data to the display from the "refresh memory" (see page 14, lines 10-13). Note, the office interprets that Rao inherently discloses reading from the "refresh memory" at a rate that supports a refresh rate of the display device as such a feature must be present in order for data to be correctly displayed on the display of Rao. Further note, the office interprets the display controller of Rao functionally equivalent to the "2D graphics engine" as Rao discloses the display controller providing a number of graphics functions such as line draws and polygon fills along with others (see page 12, lines 24-29). Note, in reference to claim 2, Rao discloses prior systems where the frame buffer (comprising the "refresh memory") is separate and apart from the system memory (see page 6, lines 22-26).

In reference to claim 9, Rao discloses all of the claim limitations as applied to claim 1 above. Rao discloses that the "screen update" and "refresh" memories are role reversed so that the previous "screen update" block now becomes the "refresh" block and the previous "refresh"

block now becomes the "frame preparation" block (see page 15, lines 8-16), therefore the office interprets that each memory block is connected to both the display controller and display device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3-8 and 10-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rao (WO 97/06523) in view of Akeley (U.S. Patent 6,075,543).

In reference to claim 3, Rao discloses all of the claim limitations as applied to claim 1 above. Although Rao discloses that the "screen update" and "refresh" memories become role reversed so that the previous "screen update" block now becomes the "refresh" block and the previous "refresh" block now becomes the "frame preparation" block (see page 15, lines 8-16), Rao does not explicitly disclose copying the color data from the frame preparation memory to the refresh memory. Akeley discloses a system and method for managing multiple frame buffers (see column 3, lines 29-30) wherein the contents of a back buffer is copied to a front buffer (see columns 4-5, lines 64-6) and where it is further displayed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the multiple buffer data transferring techniques of Akeley with the unified memory system of Rao in order to avoid the use of complicated "switching" hardware used to switch data lines between the buffers and other processing units by creating fixed data lines to/from front/back buffers to other hardware

devices. Further, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement the copying of data from "screen update" to "refresh" memories of Rao. Applicant has not disclosed that such a copying feature provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the "reversal" of roles of the "screen update" and "refresh" memories of Rao because, as Akeley states in column 5, lines 3-6, the copying and "swapping" of roles of the front and back buffers provide the same functionality and therefore are seen as a matter of design choice implementation as preferred by the designer and to which best suits the application at hand. Therefore, it would have been obvious to one of ordinary skill in this art to modify Rao to obtain the invention as specified in claim 3.

In reference to claim 4, Rao and Akeley disclose all of the claim limitations as applied to claim 3 above, in addition, Akeley discloses copying the data from the back to front buffers when a swap command is executed (see column 5, lines 12-17) which the office interprets equivalent to a predetermined interval.

In reference to claim 5, Rao and Akeley disclose all of the claim limitations as applied to claim 3 above, in addition, Akeley discloses pushing the back buffer onto a queue to be displayed (becoming the front buffer) when rendering of the back buffer is complete wherein the back buffer is then displayed on the display device (see column 5, lines 26-37).

In reference to claim 6, Rao discloses all of the claim limitations as applied to claim 1 above. Rao does not explicitly disclose further partitioning the color buffer into a third logical buffer. Akeley discloses a system and method for managing multiple frame buffers (see column

3, lines 29-30) wherein the contents of a back buffer is copied to a front buffer (see columns 4-5, lines 64-6) and where it is further displayed. Akeley discloses an alternate embodiment of the invention whereby the system comprises of three color frame buffers (see column 8, lines 55-67 and A, B, C of Figure 2). Akeley further discloses a multiplexor configured to connect one of the buffers to the display, that buffer being the oldest buffer on a FIFO queue (see column 9, lines 13-17). Note, the office interprets that Akeley inherently discloses copying data from a third buffer to a front buffer as Akeley discloses the implementations of "swapping" the roles of the buffers and copying data between buffers to be functionally equivalent (see column 5, lines 4-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the multiple buffer processing techniques with the unified memory system of Rao in order to enable a constant-frame rate application to take longer than one frame time to generate a frame without causing a frame to be dropped (see columns 1-2, lines 66-3 of Akeley).

In reference to claim 7, Rao and Akeley disclose all of the claim limitations as applied to claim 6 above. Akeley discloses a multiplexor configured to connect one of the buffers to the display, that buffer being the oldest buffer on a FIFO queue, (see column 9, lines 13-17) and disconnecting the previously attached buffer.

In reference to claim 8, Rao and Akeley disclose all of the claim limitations as applied to claim 7 above. Rao discloses that the "screen update" and "refresh" memories are role reversed so that the previous "screen update" block now becomes the "refresh" block and the previous "refresh" block now becomes the "frame preparation" block, after writes to the previous "screen update" block have been completed (see page 15, lines 8-16). Note, the office interprets Rao to inherently disclose switching the memories when the entire frame of data is ready to be

displayed as these memories are frame memories holding frames of data (see page 13, lines 12-16) as switching memories at other times other than when a full frame is ready to be displayed would not maximize memory usage and processing cycles.

In reference to claims 10 and 11, Rao discloses a processing system including a unified system/frame buffer memory collocated in a single integrated circuit or bank of circuits (see page 6, lines 18-22). Rao discloses a core logic unit that exchanges data, addresses and instructions between a CPU, display controller and the unified memory (see pages 11-12, lines 33-2). Rao further discloses that the core logic unit may be any of a number of commercially available logic chips (see page 12, lines 3-6) which the office interprets as functionally equivalent to the memory controller of applicant's claim. Rao discloses the core logic unit connected to main memory, the display subsystem and CPU (see interconnections between core logic (#103), CPU (101) and display controller (104) of Figure 1). Rao discloses the unified memory being partitioned into a system memory and a display frame buffer which is further divided into first and second frame buffer blocks (see page 13, lines 13-16 and #105, 109-111 of Figure 1). Rao further discloses one of the two frame buffer blocks to function as "refresh" memory and the other block to function as a "screen update" memory (see pages 13-14, lines 35-1 and page 14, lines 22-23) which the office interpret as functionally equivalent to the "refresh" and "frame preparation" memories respectively, of applicant's claim. Rao further discloses that the "screen update" and "refresh" memories are role reversed so that the previous "screen update" block now becomes the "refresh" block and the previous "refresh" block now becomes the "frame preparation" block (see page 15, lines 8-16), therefore the office interprets that each memory block is connected to both the display controller and display device. Rao also discloses each

block of memory to comprise of pixel data (see page 13, lines 30-32) which the office interprets equivalent to color data. Rao discloses data being written to the "screen update" memory using one CPU cycle for each word of data being written (see page 14, lines 32-34). Rao further discloses the display controller writing refresh data to the display from the "refresh memory" (see page 14, lines 10-13). Note, the office interprets that Rao inherently discloses reading from the "refresh memory" at a rate that supports a refresh rate of the display device as such a feature must be present in order for data to be correctly displayed on the display of Rao. Further note, the office interprets the display controller of Rao functionally equivalent to the "2D graphics engine" as Rao discloses the display controller providing a number of graphics functions such as line draws and polygon fills along with others (see page 12, lines 24-29). Rao does not explicitly disclose copying the color data from the frame preparation memory to the refresh memory. Akeley discloses a system and method for managing multiple frame buffers (see column 3, lines 29-30) wherein the contents of a back buffer is copied to a front buffer (see columns 4-5, lines 64-6) and where it is further displayed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the multiple buffer data transferring techniques of Akeley with the unified memory system of Rao in order to avoid the use of complicated "switching" hardware used to switch data lines between the buffers and other processing units by creating fixed data lines to/from front/back buffers to other hardware devices. Further, at the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement the copying of data from "screen update" to "refresh" memories of Rao. Applicant has not disclosed that such a copying feature provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in

the art, furthermore, would have expected Applicant's invention to perform equally well with the "reversal" of roles of the "screen update" and "refresh" memories of Rao because, as Akeley states in column 5, lines 3-6, the copying and "swapping" of roles of the front and back buffers provide the same functionality and therefore are seen as a matter of design choice implementation as preferred by the designer and to which best suits the application at hand. Therefore, it would have been obvious to one of ordinary skill in this art to modify Rao to obtain the invention as specified in claim 10. Note, in reference to claim 11, Rao discloses prior systems where the frame buffer (comprising the "refresh memory") is separate and apart from the system memory (see page 6, lines 22-26).

In reference to claim 12, Rao and Akeley disclose all of the claim limitations as applied to claim 10 above. Claim 12 is equivalent in scope to the combination of claims 3 and 5 and therefore is rejected under similar rationale.

In reference to claim 13, Rao and Akeley disclose all of the claim limitations as applied to claim 10 above. Akeley discloses copying the data from the back to front buffers when a swap command is executed (see column 5, lines 12-17) which the office interprets equivalent to a predetermined interval.

In reference to claim 14, Rao and Akeley disclose all of the claim limitations as applied to claim 10 above. Claim 14 is equivalent in scope to the combination of claims 6-8 and therefore is rejected under similar rationale. Further, Akeley discloses writing data into the buffer which is noted, by a control mechanism, as the back buffer at a current time (see column 9, lines 4-7).

In reference to claims 15 and 16, claims 15 and 16 are equivalent in scope to claims 10 and 11 respectively and are therefore rejected under similar rationale. Further, Rao discloses the system to comprise of a CPU (#101 of Figure 1), main memory connected thereto via bus lines and the core logic (#102, 103, 105 and other local buses connecting the hardware), a graphics subsystem (which the office interprets as equivalent to #104 and 106 of Figure 1) and a display device (see #107 of Figure 1 of Rao).

In reference to claim 17, Rao and Akeley disclose all of the claim limitations as applied to claim 15 above. Claim 17 is equivalent in scope to claim 4 and therefore is rejected under similar rationale.

In reference to claim 18, Rao and Akeley disclose all of the claim limitations as applied to claim 15 above. Claim 18 is equivalent in scope to claim 5 and therefore is rejected under similar rationale.

In reference to claim 19, Rao and Akeley disclose all of the claim limitations as applied to claim 15 above. Claim 19 is equivalent in scope to claim 6 and therefore is rejected under similar rationale.

In reference to claim 20, Rao and Akeley disclose all of the claim limitations as applied to claim 19 above. Claim 20 is equivalent in scope to claim 7 and therefore is rejected under similar rationale.

In reference to claim 21, Rao and Akeley disclose all of the claim limitations as applied to claim 20 above. Claim 21 is equivalent in scope to claim 8 and therefore is rejected under similar rationale.

In reference to claims 22 and 32, claims 22 and 23 are equivalent in scope to claims 10 and 11 respectively and are therefore rejected under similar rationale. Further, Rao discloses a DAC (digital-to-analog converter) that prepares the color data for display by performing color data operations such as, for example, color format conversion (see pages 12-13, lines 35-4).

In reference to claim 24, Rao and Akeley disclose all of the claim limitations as applied to claim 22 above. Claim 24 is equivalent in scope to claim 5 and therefore is rejected under similar rationale.

In reference to claim 25, Rao and Akeley disclose all of the claim limitations as applied to claim 22 above. Claim 25 is equivalent in scope to claim 4 and therefore is rejected under similar rationale.

In reference to claim 26, Rao and Akeley disclose all of the claim limitations as applied to claim 22 above. Claim 26 is equivalent in scope to claim 14 and therefore is rejected under similar rationale.

Response to Arguments

3. Applicant's arguments filed 8/02/04 have been fully considered but they are not persuasive.

In reference to applicant's arguments filed, 8/02/04, directed to claims 1, 2 and 9, the applicant argues that Rao does not teach or suggest a graphics subsystem including a 2D graphics engine, in which the graphics subsystem is coupled to the frame preparation memory (see page 11, 4th paragraph of Applicant's Arguments). This newly added limitation is recited in Rao where Rao discloses a display controller providing a number of graphics functions such as

line draws and polygon fills along with others (see page 12, lines 24-29 of Rao). Further, applicant argues that Rao does not teach mapping part of the color buffer onto a physical memory device separate from the main memory. The office has included a prior art disclosure of Rao which suggests having separate physical mapped memories. Further, the office points to Rao, page 16, lines 11-30, wherein Rao discloses the frame buffer and system memories configured in multiple banks of memory (also see #201 of Figure 2). Rao further discloses that two banks of memory #201a and #201b represent the frame buffer portions of memory which, as disclosed above, is divided into first and second blocks (see page 16, lines 11-15 and #201a,b of Figure 2). The remaining banks of memory are used for system memory, as disclosed by Rao (see page 16, lines 11-15). Rao further discloses that each of the banks are separate DRAM devices (see page 16, lines 19-20) therefore, the office interprets that Rao does in fact teach mapping part of the frame buffer onto a physical memory device separate from system memory since each of the banks of memory are separate physical devices.

In reference to applicant's arguments filed, 8/02/04, directed to claims 3-8 and 10-26, the applicant argues that the addition of the Akeley reference does not teach or suggest a graphics subsystem including a 2D graphics engine or mapping an address for the refresh memory onto a physical memory device separate from the main memory (see page 13, paragraphs 1-2 of Applicant's Remarks). The Akeley reference has been included in the rejection of the above claims in order to disclose the copying of data from buffer portions. The Rao reference discloses all of the limitations as described above and therefore, the office interprets that a *prima facie* case of obviousness has been properly made.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (703) 305-1391. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella, can be reached at (703)-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

aac

11/12/04

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600